What is claimed is:

1. A Linear Complementarity Problem (LCP) solver, comprising:

a plurality of Island Processing Engines (IPEs), wherein each IPE receives an island data set and further comprises a plurality of parallel execution units;

wherein each one of the plurality of execution units resolves a data portion derived from the island data set.

2. The LCP solver of claim 1, wherein at least one of the plurality of execution units comprises a vector processor.

3. The LCP solver of claim 1 wherein each IPE further comprises:

an IPE memory storing the island data set;

an Island Control Unit (ICU) logically controlling the transfer of data from the IPE memory to the plurality of execution units.

4. The LCP solver of claim 3 wherein each execution unit further comprises:

an associated memory storing a respective data portion.

5. The LCP solver of claim 3 wherein each IPE further comprises:

a Content Addressable Memory (CAM) operatively connected to the ICU, such that by inter-operation of the ICU and CAM each respective data portion is derived from the island data set.

6. A system executing a main application and comprising:

a Central Processing Unit (CPU), a main memory, and one or more peripherals including a display;

wherein the main memory stores an initial data set related to a physics-based problem arising from execution of the main application;

the system further comprising a Linear Complementarity Problem (LCP) solver executing a projected iterative descent method adapted to resolve LCPs derived from the initial data set using a plurality of execution units arranged in parallel.

7. The system of claim 6, wherein each one of the plurality of execution units comprises a circuit executing floating point operations.

8. The system of claim 7, wherein the initial data set is divided into a plurality of island data sets; and

wherein the LCP solver further comprises:

a plurality of Island Processing Engines (IPEs), wherein each IPE comprises a plurality of parallel execution units and an IPE memory storing one of the plurality of island data sets.

9. The system of claim 8, wherein each IPE further comprises an Island Control Unit (ICU) controlling the transfer of data from the IPE memory to the plurality of execution units.

10. The system of claim 9, wherein each one of the plurality of execution units comprises a Vector Processing Unit (VPU) having an associated VPU memory.

11. The system of claim 10, wherein each IPE further comprises:

a Content Addressable Memory (CAM) operatively connected to the ICU, such that by interoperation of the ICU and CAM respective data portions are derived from the island data set and transferred to a corresponding VPU for resolution.

12. A system executing a main application and comprising:

a Central Processing Unit (CPU), a main memory associated with the CPU, and one or more peripherals including a display;

wherein the main memory stores an initial data set related to a physics-based problem arising from execution of the main application;

the system further comprising a Physics Processing Unit (PPU), the PPU comprising:

a PPU memory receiving and storing at least a portion of the initial data set, including a plurality of island data sets, each island data set corresponding to a rigid body island defined in the initial data set; and,

a Linear Complementarity Problem (LCP) solver executing a computational method adapted to resolve a plurality of LCPs, each LCP being derived from a corresponding island data set;

wherein the LCP solver comprises a plurality of execution units resolving the plurality of LCPs in parallel.

13. The system of claim 12, wherein the LCP solver further comprises:

a plurality of Island Processing Engines (IPEs), each IPE receiving an island data set and further comprises a plurality of parallel execution units;

wherein each one of the plurality of execution units resolves a data portion derived from the island data set.

14. The system of claim 13, wherein at least one of the plurality of execution units comprises a vector processor.

15. The system of claim 13 wherein each IPE further comprises:

an IPE memory storing the island data set;

an Island Control Unit (ICU) logically controlling the transfer of data from the IPE memory to the plurality of execution units.

16. The system of claim 15 wherein each execution unit further comprises an associated memory storing a respective data portion.

17. The system of claim 16 wherein each IPE further comprises:

a Content Addressable Memory (CAM) operatively connected to the ICU, such that by inter-operation of the ICU and CAM each respective data portion is derived from the island data set.

18. The system of claim 15 wherein the PPU further comprises:

a PPU Control Engine (PCE) controlling overall operation of the PPU; and

a Data Movement Engine (DME) controlling the transfer of data between the main memory and the PPU memory and the transfer of data between the PPU memory and respective IPE memories associated with the plurality of IPEs.

19. The system of claim 18 wherein the PPU communicates data with at least one of the CPU and main memory via at least one protocol selected from a group of protocols defined by USB, USB2, Firewire, PCI, PCI-X, PCI-Express, and Ethernet.

20. The system of claim 12, wherein the PPU is implemented as a physically separate co-processor operating in conjunction with the CPU, and the LCP solver further comprises:

a plurality of Vector Processing Units (VPUs) connected in parallel and adapted to perform multiple floating point operations to simultaneously resolve the plurality of LCPs.

21. The system of claim 20, wherein the PPU is implemented on a PCI expansion board and connected within the system via a PCI expansion slot.

22. A Linear Complementarity Problem (LCP) solver implementing a projected iterative descent method adapted to resolve an LCP and comprising:

a memory storing a data set related to a physics-based problem, the data set comprising an LCP that defines a whole gradient vector; and

a plurality of execution units arranged in parallel and each receiving one of a plurality of subspaces, each subspace corresponding to a portion of the whole gradient vector.

23. The LCP solver of claim 22, further comprising:

a logic circuit defining the plurality of subspaces, and transferring each one of the subspaces to a corresponding one of the plurality of execution units;

wherein each subspace is resolved within its corresponding one of the plurality of execution units, such that the whole gradient vector is resolved by parallel resolution of the plurality of subspaces.

24. The LCP solver of claim 23, wherein the logic circuit comprises a Content Addressable Memory (CAM).

25. The LCP solver of claim 23, wherein the projected iterative descent method comprises one selected from a group consisting of a Gauss-Seidel method and a steepest descent method.